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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/085,724	02/28/2002	Moataz A. Mohamed	00CON105P	1708

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FARJAMI & FARJAMI LLP
26522 LA ALAMEDA AVENUE, SUITE 360
MISSION VIEJO, CA 92691

EXAMINER	
TSAI, HENRY	

ART UNIT	PAPER NUMBER
2183	

DATE MAILED: 07/22/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/085,724	MOHAMED ET AL.	
	Examiner	Art Unit	
	Henry W.H. Tsai	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06 May 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-3,6-8,11-15 and 18-20* is/are pending in the application.

4a) Of the above claim(s) __ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3,6-8,11-15 and 18-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on __ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless -

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1-3, 6-8, 11-15 and 18-20 are rejected under 35 U.S.C. 102(e) as being anticipated by Tremblay et al. (U.S. Patent Application Publication No. 2001/0042190) (hereafter referred to as Tremblay et al.'190).

Referring to claim 1, Tremblay et al.'190, as claimed, a VLIW processor (100, see Fig. 1) comprising: first and second register file banks (614/616 and 610/612, see Fig. 6), said first register file bank (610/612, see Fig. 6) comprising a first plurality of read ports and write ports (see Fig. 6, the read and

write ports for reading and writing the local and global registers in 610/612), and said second register file bank (614/616, see Fig. 6) comprising a second plurality of read ports and write ports (see Fig. 6, the read and write ports for reading and writing the local and global registers in 614/616); first (comprising function units 620/622, see Fig. 6) and second data path blocks (comprising function units 624/626, see Fig. 6), said first data path block comprising a first plurality of execution units (620/622, see Fig. 6), and said second data path block comprising a second plurality of execution units (624/626, see Fig. 6); a first plurality of buses (the buses for connecting the registers 610/612 to function units 620/622 see Fig. 6) coupling said first plurality of read ports to each of said first and second data path blocks; a second plurality of buses (the buses for connecting the registers 614/616 to function units 624/626 see Fig. 6) coupling said second plurality of read ports to each of said first and second data path blocks (see also paragraph [0064] lines 13-14, regarding the global registers are read by all function units 620, 622, 624, and 626); wherein an operand residing in said first plurality of read ports is concurrently accessed by said first plurality of execution units in said first data path block and by said second plurality of execution units in said second data path block (since as set forth above the

global registers are read by all function units 620, 622, 624, and 626 see also paragraph [0064] lines 13-14) and wherein a result of an operation performed in said first data path block is written to only said first plurality of write ports without being written to said second plurality of write ports (see Fig. 6, such as the results from function units GFU 620 and MFU1 622 are written to only the corresponding local registers through the write ports without being written to the write ports connecting to function units MFU2 624 and MFU3 626), wherein said VLIW processor does not include a move bus (see Fig. 6, there's no move bus between the registers 610/612 and registers 614/616).

Referring to claim 7, Tremblay et al.'190, as claimed, a VLIW processor (100, see Fig. 1) comprising: a plurality of register file banks (inside RF1, see Fig. 1), each of said plurality of register file banks (614/616 and 610/612, see Fig. 6) comprising a respective plurality of read ports and write ports; a plurality of data path blocks (620/622, and 624/626, see Fig. 6), each of said plurality of data path blocks comprising a respective plurality of execution units (function units 620/622, and 624/626, see Fig. 6); a plurality of buses (the buses for connecting the registers 610/612 to function units 620/622; and the registers 614/616 to function units 624/626 see Fig. 6)

coupling said plurality of register file banks to each of said plurality of data path blocks; wherein an operand residing in each of said respective plurality of read ports is concurrently accessed by each of said respective plurality of execution units (since as set forth above the global registers are read by all function units 620, 622, 624, and 626 see also paragraph [0064] lines 13-14), and wherein a result of an operation performed in one of said plurality of data path blocks is written to only said respective plurality of write ports (see Fig. 6, such as the results from function units GFU 620 and MFU1 622 are written to only the corresponding local registers through the write ports without being written to the write ports connecting to function units MFU2 624 and MFU3 626), wherein said VLIW processor does not include a move bus (see Fig. 6, there's no move bus between the register files 610/612 and 614/616).

Referring to claim 11, Tremblay et al.'190, as claimed, a VLIW processor (100, see Fig. 1) comprising: first and second register file banks (614/616 and 610/612, see Fig. 6), said first register file bank (610/612, see Fig. 6) comprising a first plurality of read ports and write ports, and said second register file bank comprising a second plurality of read ports and write ports; first and second data path blocks (620/622, and 624/626, see Fig. 6), said first data path block comprising a first

plurality of execution units (function units 620/622, see Fig. 6), and said second data path block comprising a second plurality of execution units (function units 624/626, see Fig. 6); a first plurality of buses (the buses for connecting the registers 610/612 to function units 620/622 see Fig. 6)coupling said first plurality of read ports to each of said first and second data path blocks; a second plurality of buses (the buses for connecting the registers 614/616 to function units 624/626 see Fig. 6) coupling said second plurality of read ports to each of said first and second data path blocks; wherein during a single clock cycle (note as a conventional processor, a read is processed during a single clock cycle in the Tremblay et al.'190's system) an operand residing in one of said first plurality of read ports (see Fig. 6, the read ports for the local registers inside 610/612 registers) is accessed by only one of said first plurality of execution units (function units GFU 620 and MFU1 622) and wherein a result of an operation performed in said first data path block is written to only said first plurality of write ports without being written to said second plurality of write ports (see Fig. 6, such as the results from function units GFU 620 and MFU1 622 are written to only the corresponding local registers through the write ports without being written to the write ports connecting to function units

MFU2 624 and MFU3 626), wherein said VLIW processor does not include a move bus (see Fig. 6, there's no move bus between the register files 610/612 and 614/616).

Referring to claim 19, Tremblay et al.'190, as claimed, a VLIW processor (100, see Fig. 1) comprising: a plurality of register file banks (614/616 and 610/612, see Fig. 6), each of said plurality of register file banks comprising a respective plurality of read ports and write ports; a plurality of data path blocks (620/622, and 624/626, see Fig. 6), each of said plurality of data path blocks comprising a respective plurality of execution units (function units 620/622, and 624/626, see Fig. 6); a plurality of buses coupling said plurality of register file banks to each of said plurality of data path blocks (see Fig. 6); wherein during a single clock cycle (note as a conventional processor, a read is processed during a single clock cycle in the Tremblay et al.'190's system) an operand residing in one of said respective plurality of read ports (see Fig. 6, such as the read ports for the local registers inside 610/612 registers) is accessed by only one (such as function units GFU 620 and MFU1 622) of said respective plurality of execution units, and wherein a result of an operation performed in one of said plurality of data path blocks is written only to said respective plurality of write ports (see Fig. 6, such as the results from

function units GFU 620 and MFU1 622 are written to only the corresponding local registers through the write ports without being written to the write ports connecting to function units MFU2 624 and MFU3 626), wherein said VLIW processor does not include a move bus (see Fig. 6, there's no move bus between the register files 610/612 and 614/616).

As to claim 2, Tremblay et al.'190 also discloses: an operand residing in said second plurality of read ports is concurrently (this is the situation when the operand is in global registers see Fig. 6) accessed by said first plurality of execution units in said first data path block and by said second plurality of execution units in said second data path block (see paragraph [0064] lines 13-14, regarding the global registers are read by all function units 620, 622, 624, and 626).

As to claims 3, 8, 15, and 20, Tremblay et al.'190 also discloses: each of said first and second plurality of execution units is selected from the group consisting of an ALU and a multiplier (see Fig. 6, such as MFU1 622 has a function to do Multiplier and add (Muladd); and MFU2 has a function to do Multiplier (Mul) and all can conduct, as an ALU, the arithmetic operations).

As to claims 6, and 18, Tremblay et al.'190 also discloses: a result of an operation performed in said second data path block

(comprising function units 624/626) is accessed only by said second plurality of write ports (the write ports for the local registers inside register files 614/616) without being accessed by said first plurality of write ports. Note this is the situation that the write ports for the local registers inside register files 614/616 access the results from the operations in 624/626 see Fig. 6.

As to claim 12, Tremblay et al.'190 also discloses: during said single clock cycle an operand residing in one of said first plurality of read ports is accessed by only one of said second plurality of execution units in said second data path block (this is the situation when only MFU2 624 or MFU3 626 reads the global registers in 610/612 and GFU 620 and MFU1 622 do not read the global registers in 610/612).

As to claim 13, Tremblay et al.'190 also discloses: during said single clock cycle an operand residing in one of said second plurality of read ports is accessed by only one of said first plurality of execution units in said first data path block (this is the situation when only GFU 620 or MFU1 622 reads the global registers in 614/616 and MFU2 624 and MFU3 626 do not read the global registers in 614/616).

As to claim 14, Tremblay et al.'190 also discloses: during said single clock cycle (note as a conventional processor, a read

is processed during a single clock cycle in the Tremblay et al.'190's system) an operand residing in one of said second plurality of read ports is accessed by only one of said second plurality of execution units in said second data path block (Note this is the situation the read ports for the local registers inside register files 614/616 are accessed by the function units 624/626 respectively since the registers are local).

Response to Arguments

3. Applicant's arguments filed 5/6/05 have been fully considered but they are not deemed to be persuasive.

Applicants argue that "Tremblay, therefore, does not teach, disclose, or suggest the VLIW processor in the present invention because the register files in Tremblay are divided into individual local and global registers, which are each written to and accessed by the functional units differently. Accordingly, the disclosure in Tremblay regarding the global registers, which are read and written to by all functional units does not teach, disclose or suggest a VLIW processor wherein the result of an operation performed in a first data path block is written to only a first plurality of write ports without being written to a

second plurality of write ports as required by independent claims 1, 7, 11, and 19" (page 10, lines 20-21 and page 11, lines 1-6). Examiner disagrees with Applicants. As set forth in the art rejections above, Tremblay et al.'190 discloses the claimed invention **comprising**: a result of an operation performed in said first data path block is written to only said first plurality of write ports without being written to said second plurality of write ports (see Fig. 6, such as the results from function units GFU 620 and MFU1 622 are written to only the corresponding local registers through the write ports without being written to the write ports connecting to function units MFU2 624 and MFU3 626), wherein said VLIW processor does not include a move bus (see Fig. 6, there's no move bus between the registers 610/612 and registers 614/616). Note the claims 1, 7, 11, and 19 are open-ended claims since "comprising" is used therein.

Applicants further argue that "Furthermore, the disclosure in Tremblay regarding the local registers, which are read only by a functional unit associated with a particular register file segment does not teach, disclose or suggest a VLIW processor wherein an operand residing in a first plurality of read ports is concurrently read by a first plurality of execution units in a first data path block and by a second plurality of execution

units in a second data path block, as required by independent claims 1, 7, 11, and 19" (page 11, lines 6-12). Examiner disagrees with Applicants. As set forth in the art rejections above, Tremblay et al.'190 discloses the claimed invention **comprising**: an operand residing in said first plurality of read ports is concurrently accessed by said first plurality of execution units in said first data path block and by said second plurality of execution units in said second data path block (since as set forth above the global registers are read by all function units 620, 622, 624, and 626 see also paragraph [0064] lines 13-14). Again, note the claims 1, 7, 11, and 19 are open-ended claims since "comprising" is used therein.

In summary, Tremblay et al.'190 anticipates the claimed invention.

Conclusion

4. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action

is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Contact Information

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dr. Henry Tsai whose telephone number is (571) 272-4176. The examiner can normally be reached on Monday-Thursday from 8:00 AM to 5:00 PM. If attempts to reach the examiner by telephone are unsuccessful, the examiner supervisor, Eddie Chan, can be reached on (571) 272-4162. Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to **the TC central telephone number, 571-272-2100.**

6. In order to reduce pendency and avoid potential delays, Group 2100 is encouraging FAXing of responses to Office actions

directly into **the Group at fax number: 571-273-8300.** This practice may be used for filing papers not requiring a fee. It may also be used for filing papers which require a fee by applicants who authorize charges to a PTO deposit account. Please identify the examiner and art unit at the top of your cover sheet. Papers submitted via FAX into Group 2100 will be promptly forward to the examiner.

HENRY W. H. TSAI
PRIMARY EXAMINER

July 14, 2005